

## REMARKS/ARGUMENTS

Applicant has reviewed the Office Action of October 2, 2006 and made amendments to the claims, as indicated hereinabove, to overcome the Examiner's objections and place the application in condition for allowance. No new matter has been added.

### RESPONSE TO AFFIDAVITS:

#### DECLARATION

Examiner indicates that the Declaration filed by the Applicant on August 15, 2006, regarding the limited battery life under 37 CFR 1.132, is insufficient to overcome the rejection of the claims based upon the combination of Altstatt (U.S. Patent 5,771,441) in view of Schotz et al (U.S. Patent 5,946,343). Since the Examiner indicated that some of the documents and data sheets were unreadable, a complete copy of the Declaration ("Declaration") with Exhibits is forwarded once again, as EXHIBIT - I. Applicant apologizes to the Examiner for any inconvenience this may have caused.

Nonetheless, in the interest of moving forward with the prosecution, Applicant has canceled those claims rejected using the combination of Altstatt (U.S. Patent 5,771,441) in view of Schotz et al (U.S. Patent 5,946,343). Specifically, Applicant cancels Claims 1-18, 35-36 and 39-40 in this amendment without prejudice and without acquiescing or agreeing to the grounds of rejection. Applicant will, however, prosecute these claims in a continuation application.

Accordingly, the issues raised in the Office Action directed to the Declaration filed by the Applicant on August 15, 2006, no longer apply to the merits of pending claims 19-34, 37-38 and 41-53.

However, since claims 1-18, 35-36, and 39-40 will be included in Applicant's continuing application, Applicant wishes to preserve his rights regarding these claims.

### SECOND DECLARATION

Examiner indicates that the second declaration ("Second Declaration") filed by the Applicant on August 15, 2006, regarding FSK and FHSS under 37 CFR 1.132, is insufficient to overcome the rejection of the new matter (See Exhibit 5 to August 15, 2006 Response).

According to the Examiner, the CDMA overview provided by [www.telecomspace.com](http://www.telecomspace.com) discloses the following three ways to spread the bandwidth of a signal in CDMA:

1) Frequency hopping (FHSS). The signal is rapidly switched between different frequencies within the hopping bandwidth pseudo-randomly, and the receiver knows before hand where to find the signal at any given time.

2) Time hopping (THSS). The signal is transmitted in short bursts pseudo-randomly, and the receiver knows beforehand when to expect the burst.

3) Direct sequence (DHSS). The digital data is directly coded at a much higher frequency. The code is generated pseudo-randomly, the receiver knows how to generate the same code, and correlates the received signal with that code to extract the data.

Examiner asserts that the Applicant discussed the two ways to spread the bandwidth (i.e. FHSS & DHSS) in the Second Declaration and since the website discusses three, FHSS and DHSS are not inherent features of CDMA.

In this regard, Applicant hereby wishes to clarify that the same website indicates that the CDMA was commercially introduced in 1995, became one of the world's fastest-growing wireless technologies, and it is a form of Direct Sequence Spread Spectrum communication. Applicant is not claiming that he invented FHSS, THSS, or DSSS. Applicant simply relied on a book entitled "Spread Spectrum Systems with Commercial Applications" by a well known author Robert C. Dixon's ("Dixon"), and the Applicant provided excerpts of some relevant pages to the Examiner to clarify the issue. The fact that the website indicated by the Examiner discusses three approaches to spread the bandwidth of the signal versus the two approaches pointed out by Dixon is irrelevant, and even if relevant, the discrepancy by two known sources can be properly explained. For example, on page 47, Dixon explains that "Simple time-hopping modulation offers little in the way of interference rejection because a continuous carrier at the signal center frequency can block communications effectively." And, this may be the reason why Dixon has not elaborated on THSS. A copy of the relevant page(s) from Dixon is attached hereto as EXHIBIT - II.

However, since Applicant has canceled the subject matter indicated in this Office Action as being new matter related to FSK and FHSS in paragraph [0010], the issue raised by the Examiner with reference to Second Declaration is moot and no longer applies to the merits of the pending claims 19-34, 37-38 and 41-53.

The Examiner points out the requirements set forth in MPEP Section 2112, which are related to rejections based on inherency. The Applicant respectfully submits that the arguments presented by the Examiner with reference to inherency appear to be

out of context. The Federal Circuit in *Kennecott Corp. v. Kyocera Intern., Inc.*, 835 F.2d 1419, 1422 (Fed.Cir.1987) held that the doctrine of inherency provides that "[b]y disclosing in a patent application a device that inherently performs a function, ..., a patent applicant necessarily discloses that function ... even though they say nothing concerning it." (emphasis added). To rely on this doctrine, the patentee must show that "the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art." *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed.Cir.2001). The same court further explained that to apply the doctrine of inherency, the party relying on the doctrine must prove that the challenged circumstance "inevitably occurs when the process steps ... are followed," *Kooi v. DeWitt*, 546 F.2d 403, 409 (Cust. & Pat.App.1976), or are "inevitable." *Application of Wilding*, 535 F.2d 631, 636 (Cust. & Pat.App.1976); see also *Kropa v. Robie*, 38 C.C.P.A. 858, 187 F.2d 150, 154-55 (Cust. & Pat.App.1951) ("Inherency does not mean that a thing might happen one out of twenty times.... It must inevitably happen for the doctrine to apply."). In sum, the doctrine of inherency is satisfied where the patent "inherently discloses the invention ... so that one skilled in the art could produce the results claimed in the [patent] simply by practicing the [patent], i.e., the result flows naturally from the express disclosures" of the patent. *Rosco, Inc. v. Mirror Lite Co.*, 139 F.Supp.2d 287 (E.D.N.Y.2001).

As stated above, [www.telecomspace.com](http://www.telecomspace.com) website indicates that the CDMA was commercially introduced in 1995, became one of the world's fastest-growing wireless technologies, and it is a form of Direct Sequence Spread Spectrum communications.

The Applicant has disclosed CDMA and explained how his invention works utilizing a unique codeword that spreads the signal spectrum. Paragraph 0014 of the parent application states that: "Modulation of the digital signal may be performed using direct sequence spread spectrum communication technology. A 64-Ary modulator 42 may be used for summation at summation element 46 with a transmitter code generator 44 signal to produce a high symbol rate, and a unique codeword that spreads the signal spectrum." (emphasis added). Paragraph 0016 of the parent application states that "This code division multiple access (CDMA) may be used to provide each user independent operation."

Based on the prosecution history, it is abundantly clear that the Applicant has disclosed the use of the CDMA technology to provide each user independent operation. The three ways to spread the bandwidth of the signal, as explained on the website, is simply a method to spread the bandwidth of the signal generated under CDMA. These methods are sub-sets of CDMA protocol. When the Applicant disclosed CDMA and explained how his invention works utilizing a unique codeword that spreads the signal spectrum, the Applicant, in essence, has disclosed all the three ways (i.e. FHSS, THSS, and DSSS) that would be so recognized by persons of ordinary skill in the relevant art. If Applicant's invention utilizes CDMA protocol, as expressly disclosed in paragraph 0016 of the parent application, it is also apparent to one skilled in the art that there are only three ways to spread the bandwidth of a signal under the CDMA (i.e. FHSS, THSS, and DSSS) and therefore these three ways are inherent features of the CDMA protocol. Without these methods for spreading bandwidth, CDMA protocol

cannot be implemented and therefore these result (i.e. methods to spread the bandwidth) flow naturally from the express disclosures of the patent application (i.e. “. . . (CDMA) may be used to provide each user independent operation.” Paragraph 0016 of the parent application).

Based on the above, Applicant respectfully requests that the Examiner withdraws his objections to the Second Declaration.

RESPONSE TO NEW MATTER REJECTIONS:

On page 6 of the Office Action, the Examiner alleges that “a unique hop pattern for each individual user” is not supported by the specification. In the interest of moving forward with the prosecution, Applicant has canceled Claims 1, 4, 6, 7 and 10-13. Specifically, Applicant cancels Claims 1-18, 35-36 and 39-40 in this amendment without prejudice and without acquiescing or agreeing to the grounds of rejection. Applicant will, however, prosecute these claims in a continuation application.

On page 6 of the Office Action, the Examiner alleges that the terms and techniques disclosed in “A frequency shift keying (FSK) modulation/detection technique could be used given a frequency hopping spread spectrum (FHSS) system choice” sentence (FSK and FHSS) were not present in the parent disclosure or in the current application’s disclosure and thus are new matter.

Nonetheless, in the interest of moving forward with the prosecution, Applicant has deleted the reference to FSK and FHSS from paragraph [0010] of the specification

without prejudice and without acquiescing or agreeing to the grounds of objection. Therefore Applicant respectfully requests that the new matter objection pertaining to the sentence "[A] frequency shift keying (FSK) modulation/detection technique could be used given a frequency hopping spread spectrum (FHSS) system choice" be withdrawn.

Since the above identified sentence has been canceled, the objection to the amendment March 14, 2006, should be withdrawn.

#### **Claim Rejections Under 35 U.S.C. §112**

The rejection of Claims 1, 4, 6, 10, 12 and 13 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement, is respectfully traversed.

As discussed above, in the interest of moving forward with the prosecution, Applicant has canceled Claims 1, 4, 6, 10, 12 and 13 without prejudice.

Based on the above, Applicant respectfully requests that the 35 U.S.C. §112 rejection of Claims 1, 4, 6, 10, 12 and 13 be withdrawn.

The rejection of Claims 19-32, 43-53 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement, is respectfully traversed.

Examiner alleges that the Claims contain the limitations directed to DSSS, which is not in the original specification nor inherent as alleged by Applicant. The Applicant has disclosed CDMA and explained how his invention works utilizing a unique codeword that spreads the signal spectrum. Paragraph 0014 of the parent application states that: "Modulation of the digital signal may be performed using direct

sequence spread spectrum communication technology.” The direct sequence spread spectrum refers to DSSS. (emphasis added).

Based on the above, Applicant respectfully submits that Claims 19-32 and 43-53, are definite and comply with the written description requirement and therefore respectfully requests that the 35 U.S.C. §112 rejection of Claims 19-32, 43-53 be withdrawn.

In view of the above remarks, since Claims 19-32, 43-53 are not rejected under any cited references, Claims 19-32 and 43-53 are allowable.

The rejection of Claims 14 and 15 under 35 U.S.C. §112, second paragraph, is respectfully traversed.

Applicant has canceled Claims 14 and 15. Based on this, Applicant respectfully requests that the 35 U.S.C. §112 rejection of Claims 14 and 15 be withdrawn.

In view of the foregoing amendments and remarks, Applicant respectfully requests withdrawal of the §112 claim rejections.

#### Claim Rejections Under 35 U.S.C. §102

The rejection of Claims 33 and 34 under 35 U.S.C. §102(e) as being anticipated by Lindemann (U.S. Patent Application 2004/0223622) is respectfully traversed.

Claim 33 recites

*...at least one module adapted to audibly reproduce said processed CDMA signal, said CDMA communication configuration providing a user with independent audio reproduction free of interference from other users or wireless devices. (Emphasis added)*



The above emphasized claim language is not taught or suggested by Lindemann. Lindemann does not address reproduction that is interference free. Furthermore, Applicant observes that Lindemann does not mention interference or address the problem identified by Applicant and thus Applicant's solution to provide *a user with independent audio reproduction free of interference from other users or wireless devices*. Instead, Lindemann is directed to digital wireless loudspeaker system and the delivery of signals to the speakers. Thus, Lindemann is not directed to a system capable of (1) providing a user with *independent audio reproduction*; and (2) *reproduction free of interference from other users or wireless devices*.

Claim 34 contains similar language. Thus, the remarks set forth above in relation to Claim 33 equally apply to Claim 34.

Accordingly, Lindemann cannot anticipate Applicant's Claims 33 and 34. For at least this reason, Applicant respectfully requests withdrawal of the rejection of Claims 33 and 34 by Lindemann under 35 U.S.C. §102(e).

Dependent Claims 37 and 41 depend directly or indirectly from independent Claim 33. Furthermore, dependent Claims 38 and 42 depend from independent Claim 34. These dependent claims contain all of the limitations of independent Claims 33 or 34, thus, any rejections under 35 U.S.C. §§102 or 103 should be withdrawn by virtue of their dependency from independent Claims 33 or 34.

**Claim Rejections Under 35 U.S.C. §103**

As stated earlier, Claims 1-18 and 35-36 and 39-40 have been canceled without prejudice in this amendment and will be filed in a continuation application. Applicant does not acquiesce or agree to the grounds of rejection of Claims 1-18; however, because they have been cancelled, the basis of rejection of these claims will not be addressed.

The rejection of Claims 37 and 38 under 35 U.S.C. §103(a) as being unpatentable by Lindemann (U.S. Patent Application 2004/0223622) in view of Schotz '343 is respectfully traversed.

Schotz '343 is relied upon for a teaching of an analog output of 20 Hz to 20 KHz. However, Schotz '343 does not teach the deficiencies of Lindemann previously described in relation to independent Claims 33 and 34. Hence, the combination of Lindemann as modified Schotz '343 does not teach all the limitations of the base Claims (33 and 34) from which Claims 37 and 38 depend.

In view of the above remarks, the rejection of Claims 37 and 38 under 35 U.S.C. §103(a) as being unpatentable by Lindemann in view of Schotz '343 should be withdrawn.

The rejection of Claims 41 and 42 under 35 U.S.C. §103(a) as being unpatentable by Lindemann (U.S. Patent Application 2004/0223622) is respectfully traversed.

Lindemann as modified by the Examiner does not teach the deficiencies described in relation to independent Claims 33 and 34. Hence, Lindemann as modified

does not teach the claimed invention since Lindemann as modified does not teach all the limitation of the base Claims (33 and 34) from which Claims 41 and 42 depend.

In view of the above remarks, the rejection of Claims 41 and 42 under 35 U.S.C. §103(a) as being unpatentable by Lindemann should be withdrawn.

**Interview Summary in Compliance with MPEP Section 713.04**

Applicant would like to thank Examiner Flanders for the courtesy extended during the Interview of January 29, 2006. During the interview, Examiner Flanders discussed the allowability of certain claims. Examiner Flanders decided to defer the decision pending review of the Supplemental Response.

**Conclusion**

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No new claims have been added. Applicant believes that the application, as presently amended, is in condition for allowance. If for any reason the Examiner finds the application other than in condition for allowance, **Applicant respectfully requests** the Examiner to call the undersigned attorney at the telephone number listed herein below to discuss any steps necessary for placing the application in condition for allowance.

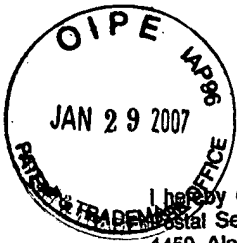
Respectfully submitted,  
THE PATEL LAW FIRM, P.C.



Nattu J. Patel  
USPTO Reg. No. 39,559

Date: January 29<sup>th</sup>, 2007

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I hereby certify that this correspondence (including Exhibits) is being deposited with the United States Postal Service via Express Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 15, 2006 (Express Mail Label No.: ET615079096US).

  
Natu J. Patel

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of C. Earl Woolfork :  
Serial No. 10/648,012 : Group Art Unit: 2615  
Confirm. No.: 3337 : Examiner: Andrew C. Flanders  
Filed: August 26, 2003 :  
For: WIRELESS DIGITAL AUDIO MUSIC SYSTEM :

**DECLARATION OF APPLICANT REGARDING LIMITED BATTERY LIFE**  
**UNDER 35 USC Section 132**

I, C. Earl Woolfork, being duly sworn, depose and declare as follows:

1. I am the Inventor of the above referenced patent application ("Application"). I have personal knowledge of the following matter and if asked to testify, could and would testify competently, thereto.
2. Daphne Burton, my then attorney, conducted the interview with Examiner Flanders and Supervisory Patent Examiner Tran (collectively "Examiners") on June 13, 2006 regarding the pending office action dated May 17, 2006. I participated in that interview.
3. During the interview, among other things, we discussed U.S. Patent No. 5,771,441 issued to Altstatt ("Altstatt" or "the 441 Patent") and U.S. Patent No. 5,946,343 issued to Schotz ("Schotz" or "the 343 Patent").
4. Examiners requested that I submit evidence in an affidavit under 35 USC Section 132 explaining as to why the combination of Altstatt in view of Schotz is non-operative due to limited battery life.
5. I am hereby submitting this affidavit and all the supporting documentation to the Examiners for their consideration.

6. Altstatt's invention is based on an analog technology and is operated by a battery. Altstatt recites that the maximum value of V is fixed by the battery voltage of 1.5 or possibly 3 volts (Column 8, lines 22-24).

7. Schotz' invention is based on digital technology. Schotz's digital wireless speaker system requires 120VAC at 60Hz. Schotz further states that "[b]oth the transmitter 22 and the receiver 24 have respective power circuits (not shown) that convert input power (e.g., 120VAC at 60 Hz) into proper voltage levels for appropriate transmitter and receiver operation." Please refer to Column 14, lines 1-4.

8. Exhibit A, attached hereto, lists the commercially available Integrated Chip components ("IC Components") that both Altstatt and Schotz identify in their respective designs. Datasheets identifying electrical current requirements to operate the IC Components are included in Exhibit B.

9. Altstatt cannot be combined with Schotz. However, even assuming such a combination is possible, the Altstatt's battery powered analog headphone system will suffer from a significantly reduced playtime due to the power consumption of Schotz's numerous integrated circuit components, as articulated in the calculation spreadsheet attached hereto as Exhibit C.

10. The "playtime" is defined as the time the invention can be operated continuously before the battery must be changed or recharged. The playtime calculation consists of simple unit conversions as defined in chapter one, problem 1.5 and solution set of well known Theodore S. Rappaport's Wireless Communications Principles & Practice textbook. The relevant pages from the textbook are attached herewith as Exhibit D.

According to Exhibit D, the formula for the playtime calculation is:

$$\{((60\text{minutes}/1\text{hour}) \times B\text{mA-h})/((60\text{ minutes}/\text{hour} \times 24\text{ hour}/\text{day})(\text{sum of IC currents in mA}))\} \times (24\text{hour}/\text{day})$$

where B is the battery current capacity.

11. As shown in Exhibit C, Altstatt's portable invention will yield a playtime greater than 10 hours when operated with a small battery having a current capacity of 50mA-h (50 milliamp-hours).

12. If we were to hypothetically apply the same 50mA-h battery capacity to operate Schotz's invention, Exhibit C further shows that the frequency hopping spread spectrum ("FHSS") system will operate for approximately six minutes, and the direct sequence spread spectrum ("DSSS") system will operate for approximately eleven

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PATENT

minutes before requiring a new battery or a recharged battery. Please note that the FHSS and DSSS system operations are constrained to the lowest device (transmitter or receiver) operation time.

Date: 4/14/06

Respectfully Submitted,

By:  C. Earl Woolfork



## EXHIBIT A

### US Patent Number: 5,771,441 Issued to Altstatt

Number	Component Description	Reference
1	Transmitter, BA1404	column 5, lines 34-37
2	Receiver, TA7766AF	column 8, lines 54-58
3	Receiver, TA7792F	column 8, lines 54-58

### US Patent Number: 5,946,343 Issued to Schotz

1	Digital Signal Processor, DSP56002	column 14, lines 49-50
2	A/D converter, SAA7360	column 7, lines 11-12
3	Stereo Filter MPEG, SAA2520	column 14, lines 47-48
4	MPEG, SAA2521	column 14, lines 47-48
5	Modulator, RF2422	column 10, lines 17-18
6	Power Amplifier, TQ9132	column 10, lines 31-32
7	Phase Locked Loop, MC12210	column 10, lines 49-50
8	Voltage Controlled Oscillator, SMV2500	column 14, lines 51-53
9	Low Noise Amplifier, MGA86576	column 11, lines 16-18
10	Digital Interface Transmitter, CS8402	column 11, lines 31-33
11	Digital to Analog Converter, TDA1305T	column 13, lines 57-59
12	Clock Recovery & Timing, TRU-050	column 12, lines 28-29
13	Demodulator, RF2703	column 12, lines 13-15
14	Microprocessor, PIC16C55	column 6, lines 63-66
15	DSSS Transmitter, CYLINK SSTX	column 16, lines 62-64
16	DSSS Receiver, CYLINK Part#SPECTRE	column 18, lines 4-5
17	Mixer, IAM81008	column 11, lines 16-18
18	Channel Encoder/Decoder, SRT241203	column 9, lines 25-26
19	Interleaver/De-interleaver, SRT-24INT	column 9, lines 50-52
20	Optical Digital Receiver, HK-3131-01	column 7, lines 40-43
21	Optical Digital Transmitter, HK-3131-03	column 13, lines 15-17
22	Voltage Controlled Oscillator, M2 D300	column 8, lines 49-50



# EXHIBIT B

US Patent Number: 5,771,441 Issued to Altstatt

Item Number 1: Transmitter, BA1404

ROHM CO LTD

40E D

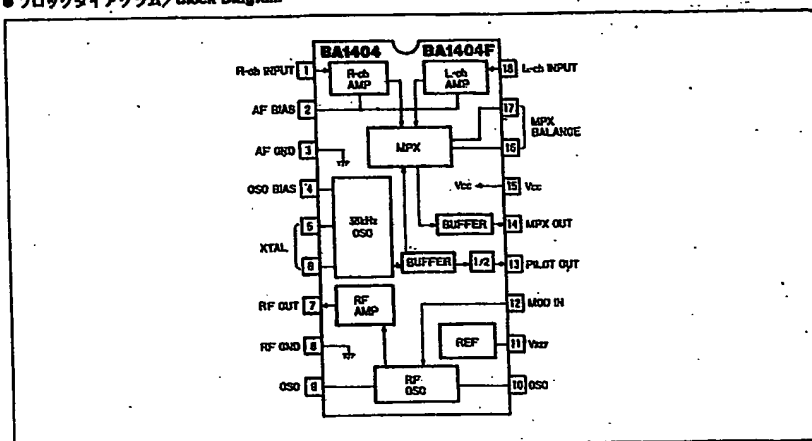
7828999 0004568 6 RHM

オーディオ用 IC/ICs for Audio Applications

BA1404/BA1404F

● ブロックダイアグラム/Block Diagram

T-77-05-05



● 絶対最大定格/Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
電源電圧	V <sub>CC</sub>	2.5	V
許容損失	P <sub>d</sub>	600*	mW
動作温度範囲	T <sub>opr</sub>	-25~75	°C
保存温度範囲	T <sub>stg</sub>	-50~125	°C

\*Ta=25°C以上で使用する場合は、1°Cにつき85mWを減じる

● 推奨動作条件/Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
電源電圧	V <sub>CC</sub>	1	1.25	2	V

● 電気的特性/Electrical Characteristics (Ta=25°C, V<sub>CC</sub>=1.25V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
経信号時電流	I <sub>Q</sub>	0.5	3	5	mA	—
入力インピーダンス	Z <sub>IN</sub>	380	640	720	Ω	f <sub>IN</sub> =1kHz
入力利得	G <sub>V</sub>	30	37	—	dB	V <sub>IN</sub> =0.5mV
チャンネルバランス	CB	—	—	2	dB	V <sub>IN</sub> =0.5mV
MPX最大出力電圧	V <sub>OM</sub>	200	—	—	mV <sub>p-p</sub>	THD≤3%
MPX 30kHzもれ	V <sub>OO</sub>	—	1	—	mV	経信号時
パイロット出力電圧	V <sub>OP</sub>	480	580	—	mV <sub>p-p</sub>	無負荷時
チャンネルセパレーション	Sep	25	45	—	dB	基準周波数にて
入力発振感度電圧	V <sub>RIN</sub>	—	1	—	μV <sub>rms</sub>	30kHz停止時 IHF-A
RF部最大出力電圧	V <sub>OSO</sub>	350	600	—	mV <sub>rms</sub>	—

ROHM

1149

オーディオ用



オーディオ用 IC/ICs for Audio Applications

ELECTRICAL CHARACTERISTICS (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 1.5\text{V}$ ,  $f_m = 1\text{kHz}$ )

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current		$I_{CC}$	—	At lamp off	—	0.8	1.6	mA
Input Resistance		$R_{IN}$	—		—	36	—	k $\Omega$
Output Resistance		$R_{OUT}$	—		—	15	—	k $\Omega$
Max. Composite Signal Input Voltage		$V_{in}(\text{MAX})$ (STEREO)	—	$L + R = 90\%$ , $P = 10\%$ , $\text{THD} = 5\%$ $\text{SW}_1 \rightarrow R_{LED} = 50\text{k}\Omega$ $\text{SW}_5 \rightarrow \text{LPF ON}$	—	250	—	mV <sub>rms</sub>
Separation		Sep	—	$L + R = 90\text{mV}_{rms}$ , $f_m = 100\text{Hz}$	—	30	—	dB
				$P = 10\text{mV}_{rms}$ , $f_m = 1\text{kHz}$	22	35	—	
				$\text{SW}_1 \rightarrow R_{LED} = 50\text{k}\Omega$ , $f_m = 10\text{kHz}$	—	30	—	
Total Harmonic Distortion	Monaural	THD (MONAURAL)	—	$V_{in} = 100\text{mV}_{rms}$ $\text{SW}_1 \rightarrow R_{LED} = 500\Omega$	—	0.2	1.5	%
	Stereo	THD (STEREO)	—	$L + R = 90\text{mV}_{rms}$ , $P = 10\text{mV}_{rms}$ $\text{SW}_1 \rightarrow R_{LED} = 50\text{k}\Omega$ $\text{SW}_5 \rightarrow \text{LPF ON}$	—	0.4	—	
Voltage Gain		$G_V$	—	$V_{in} = 100\text{mV}_{rms}$ $\text{SW}_1 \rightarrow R_{LED} = 500\Omega$	-4	-2	1	dB
Channel Balance		CB	—	$V_{in} = 100\text{mV}_{rms}$ $\text{SW}_1 \rightarrow R_{LED} = 500\Omega$	—	0	2.0	dB
Lamp ON Sensitivity		$V_L(\text{ON})$	—	Pilot input $\text{SW}_1 \rightarrow R_{LED} = 50\text{k}\Omega$	—	—	5	mV <sub>rms</sub>
Lamp OFF Sensitivity		$V_L(\text{OFF})$			7	—	—	
Stereo Lamp Hysteresis		$V_H$	—	to turn-off from turn-on	—	3	—	mV <sub>rms</sub>
Capture Range		CR	—	$P = 10\text{mV}_{rms}$	—	$\pm 3$	—	%
Carrier Leak (Note)	19kHz	CL	—	$L + R = 90\text{mV}_{rms}$ $P = 10\text{mV}_{rms}$ $\text{SW}_1 \rightarrow R_{LED} = 50\text{k}\Omega$	—	30	—	dB
	38kHz				—	50	—	
SCA Rejection Ratio		SCA Rej	—	$P = 10\text{mV}_{rms}$ , $L + R = 80\text{mV}_{rms}$ $\text{SCA} = 10\text{mV}_{rms}$ , $f_{SCA} = 67\text{kHz}$ $\text{SW}_1 \rightarrow R_{LED} = 50\text{k}\Omega$	—	70	—	dB
Signal To Noise Ratio		S/N	—	$V_{in} = 100\text{mV}_{rms}$ , $R_g = 620\Omega$ $\text{SW}_1 \rightarrow R_{LED} = 500\Omega$	—	65	—	dB

(Note) Carrier leak of 38kHz is only carrier.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>CC</sub>	5	V
Power Dissipation	TA7792P	750	mW
	TA7792F	350	
Operating Temperature	T <sub>opr</sub>	-25~75	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

(Note) Derated above Ta = 25°C in the proportion of 6mW/°C for TA7792P, and of 2.8mW/°C for TA7792F.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, Ta = 25°C, V<sub>CC</sub> = 1.5V

FM : V<sub>in</sub> = 60dBμV EMF, f = 83MHz, f<sub>m</sub> = 1kHz, Δf = ±22.5kHz

AM : V<sub>in</sub> = 60dBμV EMF, f = 1MHz, f<sub>m</sub> = 1kHz, MOD = 30%

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I <sub>CC</sub> (FM)	1	V <sub>in</sub> = 0	—	4.0	5.2	mA
	I <sub>CC</sub> (AM)	1	V <sub>in</sub> = 0	—	1.2	1.8	
FM	Input Limiting Voltage	1	V <sub>in</sub> (lim)	—	10	16	dBμV EMF
	Total Harmonic Distortion	1	THD (FM)	—	0.25	—	%
	Signal To Noise Ratio	1	S/N (FM)	—	62	—	dB
	Quiescent Sensitivity	1	Q <sub>S</sub>	—	12	—	dBμV EMF
	AM Rejection Ratio	1	AMR	—	30	—	dB
	Oscillator Voltage	2	V <sub>osc</sub>	53	90	135	mV <sub>rms</sub>
	Oscillator Stop Supply Voltage	1	V <sub>stop</sub> (FM)	—	0.85	0.95	V
	Recovered Output Voltage	1	V <sub>OD</sub> (FM)	28	45	68	mV <sub>rms</sub>
AM	Voltage Gain	1	G <sub>V</sub>	14	25	50	mV <sub>rms</sub>
	Recovered Output Voltage	1	V <sub>OD</sub> (AM)	25	40	60	mV <sub>rms</sub>
	Total Harmonic Distortion	1	THD (AM)	—	1.5	—	%
	Signal To Noise Ratio	1	S/N (AM)	—	40	—	dB
	Oscillator Stop Supply Voltage	1	V <sub>stop</sub> (AM)	—	0.85	0.95	V
Output Resistance Pin®	FM	R <sub>O</sub> (FM)	f = 1kHz	—	1.4	—	kΩ
	AM	R <sub>O</sub> (AM)	f = 1kHz	—	8	—	

※ V<sub>in</sub> : Open Display

## DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage					
• EXTAL	$V_{IHC}$	4.0	—	$V_{CC}$	V
• RESET	$V_{IHR}$	2.5	—	$V_{CC}$	V
• MODA, MODB, MODC	$V_{IHM}$	3.5	—	$V_{CC}$	V
• All other inputs	$V_{IH}$	2.0	—	$V_{CC}$	V
Input Low Voltage					
• EXTAL	$V_{ILC}$	-0.5	—	0.6	V
• MODA, MODB, MODC	$V_{ILM}$	-0.5	—	2.0	V
• All other inputs	$V_{IL}$	-0.5	—	0.8	V
Input Leakage Current EXTAL, RESET, MODA/IRQA, MODB/IRQB, MODC/NMI, DR, BR, WT, CKP, PINIT, MCBG, MCBCLR, MCCLK, D20IN	$I_{IN}$	-1	—	1	$\mu A$
Tri-state (Off-state) Input Current (@ 2.4 V/0.4 V)	$I_{TSI}$	-10	—	10	$\mu A$
Output High Voltage ( $I_{OH} = -0.4$ mA)	$V_{OH}$	2.4	—	—	V
Output Low Voltage ( $I_{OL} = 3.0$ mA) HREQ $I_{OL} = 6.7$ mA, TXD $I_{OL} = 6.7$ mA	$V_{OL}$	—	—	0.4	V
Internal Supply Current at 40 MHz <sup>1</sup>					
• In Wait mode <sup>2</sup>	$I_{CCI}$	—	90	105	mA
• In Stop mode <sup>2</sup>	$I_{CCW}$	—	12	20	mA
	$I_{CCS}$	—	2	95	$\mu A$
Internal Supply Current at 66 MHz <sup>1</sup>					
• In Wait mode <sup>2</sup>	$I_{CCI}$	—	95	130	mA
• In Stop mode <sup>2</sup>	$I_{CCW}$	—	15	25	mA
	$I_{CCS}$	—	2	95	$\mu A$
Internal Supply Current at 80 MHz <sup>1</sup>					
• In Wait mode <sup>2</sup>	$I_{CCI}$	—	115	160	mA
• In Stop mode <sup>2</sup>	$I_{CCW}$	—	18	30	mA
	$I_{CCS}$	—	2	95	$\mu A$
PLL Supply Current <sup>3</sup>					
• 40 MHz		—	1.0	1.5	mA
• 66 MHz		—	1.1	1.5	mA
• 80 MHz		—	1.2	1.8	mA
CKOUT Supply Current <sup>4</sup>					
• 40 MHz		—	14	20	mA
• 66 MHz		—	28	35	mA
• 80 MHz		—	34	42	mA
Input Capacitance <sup>5</sup>	$C_{IN}$	—	10	—	pF
Notes: 1. <b>Section 4 Design Considerations</b> describes how to calculate the external supply current. 2. In order to obtain these results all inputs must be terminated (i.e., not allowed to float). 3. Values are given for PLL enabled. 4. Values are given for CKOUT enabled. 5. Periodically sampled and not 100% tested					

### Bitstream conversion ADC for digital audio systems

SAA7360

Table 1 Output data formats

ODF2	ODF1	MODE
0	0	test
0	1	format 1
1	0	format 2
1	1	I <sup>2</sup> S

#### Reset

When pin **RESET** is held LOW the data outputs are set to zero. The **RESET** pin operates as a Schmitt trigger, enabling a power-on reset function by using an external RC circuit.

#### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DDA</sub>	analog supply voltage	note 1	-0.5	+6.5	V
V <sub>I</sub>	DC input voltage		-0.5	+6.5	V
I <sub>IK</sub>	DC input diode current		-	±20	mA
V <sub>O</sub>	DC output voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>O</sub>	DC output source or sink current		-	±20	mA
I <sub>DD</sub> or I <sub>SS</sub>	total DC V <sub>DD</sub> or V <sub>SS</sub> current		-	±0.5	A
T <sub>amb</sub>	operating ambient temperature		-40	+85	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C
V <sub>es</sub>	electrostatic handling	note 2	-2000	+2000	V
		note 3	-200	+200	V

#### Notes

1. All V<sub>DD</sub> and V<sub>SS</sub> pins must be externally connected to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

#### CHARACTERISTICS

V<sub>DD</sub> = 5 V; T<sub>amb</sub> = 25 °C; f<sub>xtal</sub> = 256f<sub>s</sub>; f<sub>s</sub> = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
V <sub>DDA</sub>	analog supply voltage		4.5	5.0	5.5	V
I <sub>DDA</sub>	analog supply current		-	43	-	mA
V <sub>DDD</sub>	digital supply voltage		4.5	5.0	5.5	V
I <sub>DDD</sub>	digital supply current		-	50	-	mA
P <sub>tot</sub>	total power consumption		-	465	-	mW

Stereo filter and codec for MPEG layer 1  
audio applications

SAA2520

## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	supply voltage		-0.5	6.5	V
$V_I$	input voltage	note 1	-0.5	$V_{DD} + 0.5$	V
$I_{SS}$	supply current from $V_{SS}$		-	160	mA
$I_{DD}$	supply current in $V_{DD}$		-	160	mA
$I_I$	input current		-10	10	mA
$I_O$	output current		-20	20	mA
$P_{tot}$	total power dissipation		-	880	mW
$T_{stg}$	storage temperature range		-55	150	°C
$T_{amb}$	operating ambient temperature range		-40	85	°C
$V_{es1}$	electrostatic handling	note 2	-1500	1500	V
$V_{es2}$	electrostatic handling	note 3	-70	70	V

## Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified
2. Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  series resistor
3. Equivalent to discharging a 200 pF capacitor through a 0  $\Omega$  series resistor.

## DC CHARACTERISTICS

 $T_{amb} = -40$  to  $85$  °C;  $V_{DD} = 3.8$  to  $5.5$  V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{DD}$	supply voltage range		3.8	5.0	5.5	V
$I_{DD}$	operating current	$V_{DD} = 5$ V (note 1)	-	82	110	mA
$I_{DD}$	operating current	$V_{DD} = 3.8$ V (note 1)	-	58	80	mA
<b>Inputs URDA, SBDIR, SBEF, LTCLK, LTCNT0, LTNCT1, X22IN, X24IN</b>						
$V_{IH}$	HIGH level input voltage		$0.7V_{DD}$	-	-	V
$V_{IL}$	LOW level input voltage		-	-	$0.3V_{DD}$	V
$-I_I$	input current	$V_I = 0$ V; $T_{amb} = 25$ °C	-	-	10	$\mu$ A
$+I_I$	input current	$V_I = 5.5$ V; $T_{amb} = 25$ °C	-	-	10	$\mu$ A
<b>Inputs PWRDWN, LTENA</b>						
$V_{IH}$	HIGH level input voltage		$0.7V_{DD}$	-	-	V
$V_{IL}$	LOW level input voltage		-	-	$0.3V_{DD}$	V
$+I_I$	input current	$V_I = V_{DD}$ ; $T_{amb} = 25$ °C	40	-	250	$\mu$ A

# Masking threshold processor for MPEG layer 1 audio compression applications

SAA2521

**DC CHARACTERISTICS** $V_{DD} = 3.8$  to  $5.5$  V;  $T_{amb} = -40$  to  $85$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{DD}$	supply voltage range		3.8	5	5.5	V
$I_{DD}$	operating current	$V_{DD} = 3.8$ V	–	15	30	mA
$I_{DD}$	operating current	$V_{DD} = 5$ V	–	25	50	mA
$I_{PWRDWN}$	stand-by current	in power-down mode	–	100	–	µA
<b>Inputs</b>						
$V_{IL}$	LOW level input voltage		0	–	$0.3 V_{DD}$	V
$V_{IH}$	HIGH level input voltage		$0.7 V_{DD}$	–	$V_{DD}$	V
$I_i$	input current		–	–	10	µA
<b>Outputs</b>						
$V_{OL}$	LOW level output voltage	note 1	–	–	0.4	V
$V_{OH}$	HIGH level output voltage	note 1	$V_{DD} - 0.5$	–	–	V
<b>3-state outputs</b>						
$I_{oz}$	OFF state current	$V_i = 0$ to $5.5$ V	–	–	10	µA

**Note**

- Maximum load current for LTDATA, LTCNT1C, LTCNT0C, LTENC, LTCLKC, TEST1, TEST2, FDAC, FDAF = 2 mA;  
for LTDATAAC = 3 mA.

**RF2422****Absolute Maximum Ratings**

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.5	V <sub>DC</sub>
Input LO and RF Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

**Caution!** ESD sensitive device.

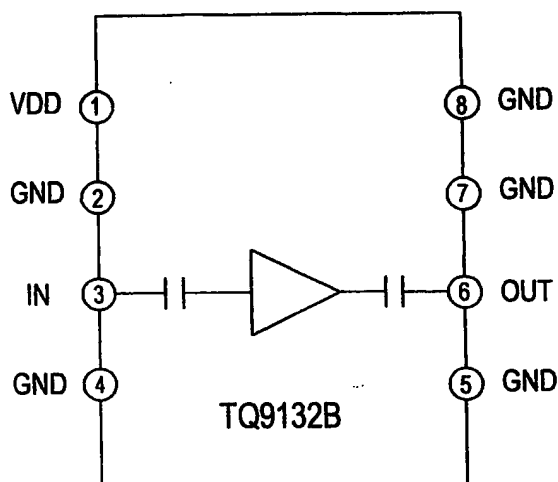
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Carrier Input</b>					T=25°C, V <sub>CC</sub> =5V
Frequency Range	800		2500	MHz	
Power Level	-6		+6	dBm	
Input VSWR		5:1 1.8:1 1.2:1			At 900MHz At 1800MHz At 2500MHz
<b>Modulation Input</b>					
Frequency Range	DC		250	MHz	
Reference Voltage (V <sub>REF</sub> )	2.0	3.0		V	
Maximum Modulation (I&Q)			V <sub>REF</sub> ±1.0	V	
Gain Asymmetry		0.2		dB	
Quadrature Phase Error		3		°	
Input Resistance		30		kΩ	
Input Bias Current			40	μA	
<b>RF Output</b>					LO=2GHz and -5dBm, I&Q=2.0V <sub>PP</sub> SSB
Output Power	-3		+3	dBm	
Output Impedance		50		Ω	
Output VSWR		3.5:1 1.3:1 1.15:1			At 900MHz At 2000MHz At 2500MHz
Harmonic Output	-30	-35		dBc	
Sideband Suppression	25	35		dB	
Carrier Suppression	30	35		dB	
IM <sub>3</sub> Suppression	30	35		dB	Intermodulation of the carrier and the desired RF signal
	25	30		dB	Intermodulation of baseband signals
Broadband Noise Floor					At 20MHz offset, V <sub>CC</sub> =5V.
		-145 -152		dBm/Hz dBm/Hz	Tied to V <sub>REF</sub> : ISIG, QSIG, IREF, and QREF. At 850MHz At 1900MHz
<b>Power Down</b>					
Turn On/Off Time			100	ns	
PD Input Resistance	50			kΩ	
Power Control "ON"			2.8	V	Threshold voltage
Power Control "OFF"	1.0	1.2		V	Threshold voltage
<b>Power Supply</b>					
Voltage		5		V	Specifications
	4.5		6.0	V	Operating Limits
Current		45	50	mA	Operating
			25	μA	Power Down



# TriQuint

SEMICONDUCTOR  
WIRELESS COMMUNICATIONS DIVISION



## Product Description

The TQ9132B amplifier is an 800-2500 MHz amplifier capable of providing moderate output power (50 mW) for a wide variety of transmit and receive applications. The amplifier's input and output are matched to 50  $\Omega$  with internal circuitry, simplifying interfaces to 50  $\Omega$  systems. In addition, DC blocking capacitors are included on chip, permitting direct connections to the input and output. Its 8-pin surface mount package and low cost are well suited to many wireless communications applications.

## Electrical Specifications<sup>1</sup>

Parameter	Min	Typ	Max	Units
Gain	13.5	16		dB
Output 1 dB Gain Compression	15.5	17		dBm
Input Return Loss		12		dB
Output Return Loss		12		dB
DC Supply Current		85	100	mA

Note 1: Test Conditions:  $V_{DD} = 5.0$  V, Freq. = 2500 MHz,  $T_A = 25^\circ$  C.

Note 2: Min/max values 100% production tested

## TQ9132B

### DATA SHEET

## 3V Cellular TDMA/AMPS Power Amplifier IC

### Features

- Single 3V- 6V supply
- Wide frequency range
- +17 dBm output power
- Input and output matched to 50  $\Omega$
- SO-8 surface mount plastic package

### Applications

- Power Amplifier drivers
- PCN Medium-power amplifiers
- Medium-power WLANs
- CDPD Modems
- Base Station receivers

ELECTRICAL CHARACTERISTICS ( $V_{CC} = 2.7$  to  $5.5$  V;  $T_A = -40$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for $V_{CC}$	$I_{CC}$	—	8.8	13.0	mA	Note 1
		—	10.2	16.0		Note 2
Supply Current for $V_p$	$I_p$	—	0.7	1.1	mA	Note 3
		—	0.8	1.3		Note 4
Operating Frequency	$f_{INmax}$ $f_{INmin}$	2500 —	— —	— 500	MHz	Note 5
Operating Frequency (OSCin)	$F_{OSC}$	—	12	20	MHz	Crystal Mode
		—	—	40	MHz	External Reference Mode
Input Sensitivity	$f_{IN}$ $OSCin$	$V_{IN}$ $V_{OSC}$	200 500	— 2200	mVpp mVpp	
Input HIGH Voltage	CLK, DATA, LE, FC	$V_{IH}$	$0.7 V_{CC}$	—	V	
Input LOW Voltage	CLK, DATA, LE, FC	$V_{IL}$	—	$0.3 V_{CC}$	V	$V_{CC} = 5.5$ V
Input HIGH Current (DATA and CLK)		$I_{IH}$	—	1.0	$\mu\text{A}$	$V_{CC} = 5.5$ V
Input LOW Current (DATA and CLK)		$I_{IL}$	—10	—5.0	$\mu\text{A}$	$V_{CC} = 5.5$ V
Input Current (OSCin)		$I_{OSC}$	— —	130 —310	$\mu\text{A}$	$OSCin = V_{CC}$ $OSCin = V_{CC} - 2.2$ V
Input HIGH Current (LE and FC)		$I_{IH}$	—	1.0	$\mu\text{A}$	
Input LOW Current (LE and FC)		$I_{IL}$	—75	—60	$\mu\text{A}$	
Charge Pump Output Current Do and BISW		$I_{Source}^6$	—2.6	—2.0	—1.4	mA $V_{DO} = V_p/2$ ; $V_p = 2.7$ V $V_{BISW} = V_p/2$ ; $V_p = 2.7$ V $0.5 < V_{DO} < V_p - 0.5$ $0.5 < V_{BISW} < V_p - 0.5$
		$I_{Sink}^6$	+1.4	+2.0	+2.6	
		$I_{Hi-Z}$	—15	—	+15	
Output HIGH Voltage (LD, $\phi_R$ , $\phi_P$ , $f_{OUT}$ )		$V_{OH}$	4.4	—	—	$V_{CC} = 5.0$ V
			2.4	—	—	$V_{CC} = 3.0$ V
Output LOW Voltage (LD, $\phi_R$ , $\phi_P$ , $f_{OUT}$ )		$V_{OL}$	—	—	0.4	$V_{CC} = 5.0$ V
			—	—	0.4	$V_{CC} = 3.0$ V
Output HIGH Current (LD, $\phi_R$ , $\phi_P$ , $f_{OUT}$ )		$I_{OH}$	—1.0	—	—	
Output LOW Current (LD, $\phi_R$ , $\phi_P$ , $f_{OUT}$ )		$I_{OL}$	1.0	—	—	

1.  $V_{CC} = 3.3$  V, all outputs open.2.  $V_{CC} = 5.5$  V, all outputs open.3.  $V_p = 3.3$  V, all outputs open.4.  $V_p = 6.0$  V, all outputs open.5. AC coupling,  $F_{IN}$  measured with a 1000 pF capacitor.

6. Source current flows out of the pin and sink current flows into the pin.

Figure 8. Typical External Charge Pump Circuit

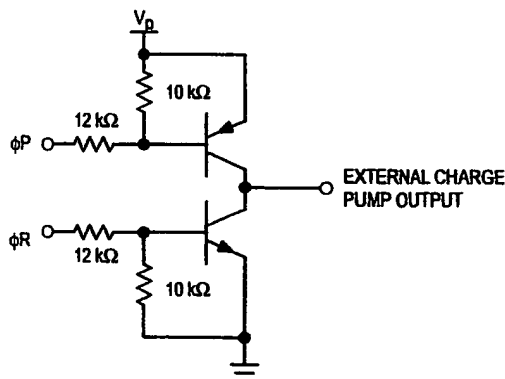
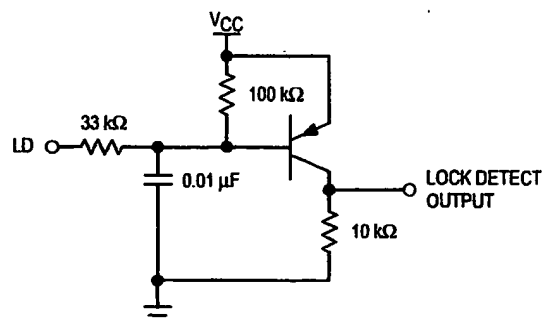


Figure 9. Typical Lock Detect Circuit





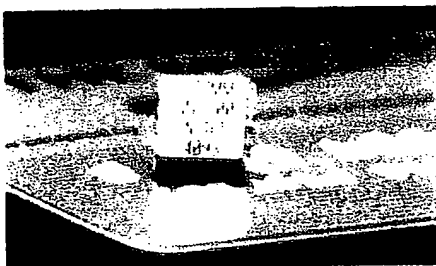
**Z-Communications, Inc.**

9939 Via Pasar • San Diego, CA 92126  
TEL (619) 621-2700 FAX (619) 621-2722

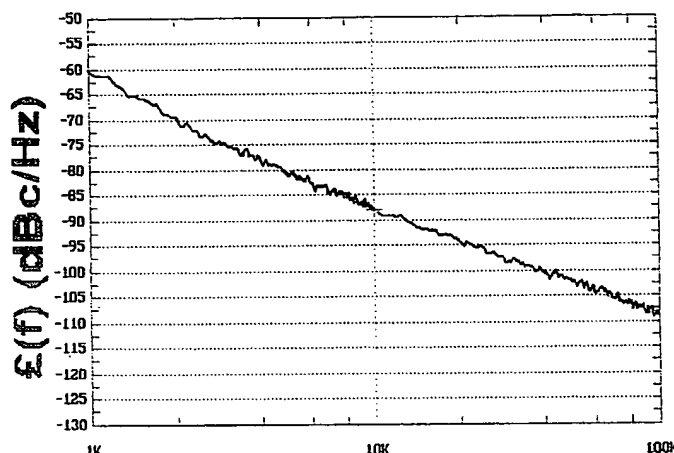
Item Number 8: Voltage Controlled Oscillator, SMV2500

**SMV2500L**

VOLTAGE CONTROLLED OSCILLATOR  
Rev E5



**PHASE NOISE (1 Hz BW, typical)**



**OFFSET (Hz)**

**FEATURES**

- Frequency Range: 2400 - 2484 MHz
- Tuning Voltage: 0-3 Vdc
- SUB-L - 8-pin Package

**APPLICATIONS**

- Personal Communications Systems
- WLAN
- Portable Radios

**PERFORMANCE SPECIFICATIONS**

	VALUE	UNITS
Oscillation Frequency Range	2400 - 2484	MHz
Phase Noise @ 10 kHz offset (1 Hz BW, typ.)	-87	dBc/Hz
Harmonic Suppression (2nd, typ.)	-20	dBc
Tuning Voltage	0-3	Vdc
Tuning Sensitivity (avg.)	105	MHz/V
Power Output	9.25±2.75	dBm
Load Impedance	50	$\Omega$
Input Capacitance (max.)	50	pF
Pushing	<30	MHz/V
Pulling (14 dB Return Loss, Any Phase)	<25	MHz
Operating Temperature Range	-40 to 85	°C
Package Style	SUB-L	

**POWER SUPPLY REQUIREMENTS**

Supply Voltage (Vcc, nom.)	3	Vdc
Supply Current (Icc, typ.)	19	mA

All specifications are typical unless otherwise noted and subject to change without notice.

**APPLICATION NOTES**

- AN-100/1 : Mounting and Grounding of VCOs
- AN-102 : Proper Output Loading of VCOs
- AN-107 : How to Solder Z-COMM VCOs

**NOTES:**

### Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum <sup>(1)</sup>
$V_d$	Device Voltage, RF output to ground	V	9
$V_g$	Device Voltage, RF input to ground	V	+0.5 -1.0
$P_{in}$	CW RF Input Power	dBm	+13
$T_{ch}$	Channel Temperature	°C	150
$T_{STG}$	Storage Temperature	°C	-65 to 150

### Thermal Resistance<sup>(2)</sup>:

$$\theta_{ch-c} = 110^{\circ}\text{C/W}$$

### Notes:

1. Operation of this device above any one of these limits may cause permanent damage.
2.  $T_c = 25^{\circ}\text{C}$  ( $T_c$  is defined to be the temperature at the package pins where contact is made to the circuit board).

### MGA-86576 Electrical Specifications, $T_c = 25^{\circ}\text{C}$ , $Z_0 = 50\ \Omega$ , $V_d = 5\ \text{V}$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$G_p$	Power Gain ( $ S_{21} ^2$ ) $f = 1.5\ \text{GHz}$ $f = 2.5\ \text{GHz}$ $f = 4.0\ \text{GHz}$ $f = 6.0\ \text{GHz}$ $f = 8.0\ \text{GHz}$	dB	20	21.2 23.7 23.1 19.3 15.4	
$NF_{50}$	50 $\Omega$ Noise Figure $f = 1.5\ \text{GHz}$ $f = 2.5\ \text{GHz}$ $f = 4.0\ \text{GHz}$ $f = 6.0\ \text{GHz}$ $f = 8.0\ \text{GHz}$	dB		2.2 1.9 2.0 2.3 2.5	2.3
$NF_o$	Optimum Noise Figure (Input tuned for lowest noise figure) $f = 1.5\ \text{GHz}$ $f = 2.5\ \text{GHz}$ $f = 4.0\ \text{GHz}$ $f = 6.0\ \text{GHz}$ $f = 8.0\ \text{GHz}$	dB		1.6 1.5 1.6 1.8 2.1	
$P_{1dB}$	Output Power at 1 dB Gain Compression $f = 1.5\ \text{GHz}$ $f = 2.5\ \text{GHz}$ $f = 4.0\ \text{GHz}$ $f = 6.0\ \text{GHz}$ $f = 8.0\ \text{GHz}$	dBm		6.4 7.0 6.3 4.3 3.8	
$IP_3$	Third Order Intercept Point $f = 4.0\ \text{GHz}$	dBm		16.0	
VSWR	Input VSWR $f = 1.5\ \text{GHz}$ $f = 2.5\ \text{GHz}$ $f = 4.0\ \text{GHz}$ $f = 6.0\ \text{GHz}$ $f = 8.0\ \text{GHz}$			3.6:1 3.3:1 2.2:1 1.4:1 1.2:1	3.6:1
	Output VSWR $f = 1.5\ \text{GHz}$ $f = 2.5\ \text{GHz}$ $f = 4.0\ \text{GHz}$ $f = 6.0\ \text{GHz}$ $f = 8.0\ \text{GHz}$			2.5:1 2.1:1 1.7:1 1.4:1 1.3:1	
$I_d$	Device Current	mA	9	16	22



CS8401A CS8402A

# **ABSOLUTE MAXIMUM RATINGS** (GND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supply	VD+		6.0	V
Input Current, Any Pin Except Supply <span style="float: right;">Note 1</span>	I <sub>in</sub>	-	±10	mA
Digital Input Voltage	V <sub>IND</sub>	-0.3	VD+	V
Ambient Operating Temperature (power applied)	T <sub>A</sub>	-55	125	°C
Storage Temperature	T <sub>stg</sub>	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

# **RECOMMENDED OPERATING CONDITIONS**

(GND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
DC Voltage	VD+	4.5	5.0	5.5	V
Supply Current <span style="float: right;">Note 2</span>	I <sub>DD</sub>		1.5	5	mA
Ambient Operating Temperature: CS8401/2A-CP or -CS <span style="float: right;">Note 3</span>	T <sub>A</sub>	0	25	70	°C
CS8401/2A-IP or -IS		-40		85	°C
Power Consumption <span style="float: right;">Note 2</span>	P <sub>D</sub>		7.5	25	mW

Notes: 2. Drivers open (unloaded). The majority of power is used in the load connected to the drivers.  
3. The '-CP' and '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only.  
The '-IP' and '-IS' parts are tested over the full -40 to 85 °C temperature range.

# **DIGITAL CHARACTERISTICS**

(T<sub>A</sub> = 25 °C for suffixes 'CP' & 'CS', T<sub>A</sub> = -40 to 85 °C for 'IP' & 'IS'; VD+ = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V <sub>IH</sub>	2.0		V <sub>DD</sub> +0.3	V
Low-Level Input Voltage	V <sub>IL</sub>	-0.3		+0.8	V
High-Level Output Voltage (I <sub>O</sub> = 200µA)	V <sub>OH</sub>	V <sub>DD</sub> -1.0			V
Low-Level Output Voltage (I <sub>O</sub> = 3.2mA)	V <sub>OL</sub>			0.4	V
Input Leakage Current	I <sub>in</sub>		1.0	10	µA
Master Clock Frequency: CS8401A <span style="float: right;">Note 4</span>	MCK			22	MHz
CS8402A <span style="float: right;">Note 4</span>				7.1	MHz
Master Clock Duty Cycle CS8401/2A		40		60	%

Notes: 4. MCK for the CS8401 must be 128, 192, 256, or 384x the input word rate based on M0 and M1 in control register 2. MCK for the CS8402A must be 128x the input word rate, except in Transparent Mode where MCK is 256x the input word rate.

Specifications are subject to change without notice.

Stereo 1fs data input up-sampling filter with  
bitstream continuous dual DAC (BCC-DAC2)

TDA1305T

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	digital supply voltage	note 1	3.4	5.0	5.5	V
V <sub>DDA</sub>	analog supply voltage	note 1	3.4	5.0	5.5	V
V <sub>DDO</sub>	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I <sub>DD</sub>	digital supply current	V <sub>DD</sub> = 5 V; at code 00000H	—	30	—	mA
I <sub>DDA</sub>	analog supply current	V <sub>DDA</sub> = 5 V; at code 00000H	—	5.5	8	mA
I <sub>DDO</sub>	operating amplifier supply current	V <sub>DDO</sub> = 5 V; at code 00000H	—	6.5	9	mA
V <sub>FS(rms)</sub>	full-scale output voltage (RMS value)	V <sub>DD</sub> = V <sub>DDA</sub> = V <sub>DDO</sub> = 5 V	1.425	1.5	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	—	−90	−81	dB
			—	0.003	0.009	%
		at −60 dB signal level	—	−44	−40	dB
			—	0.63	0.1	%
		at −60 dB signal level; A-weighted	—	−46	—	dB
S/N	signal-to-noise ratio at bipolar zero	A-weighting; at code 00000H	100	108	—	dB
BR <sub>ns</sub>	input bit rate at data input	f <sub>s</sub> = 48 kHz; normal speed	—	—	3.072	Mbits
BR <sub>ds</sub>	input bit rate at data input	f <sub>s</sub> = 48 kHz; double speed	—	—	6.144	Mbits
f <sub>sys</sub>	system clock frequency		6.4	—	18.432	MHz
TC <sub>FS</sub>	full scale temperature coefficient at analog outputs (VOL and VOR)		—	±100 × 10 <sup>−6</sup>	—	
T <sub>amb</sub>	operating ambient temperature		−30	—	+85	°C

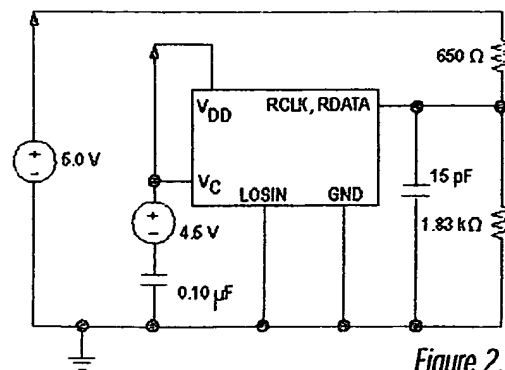
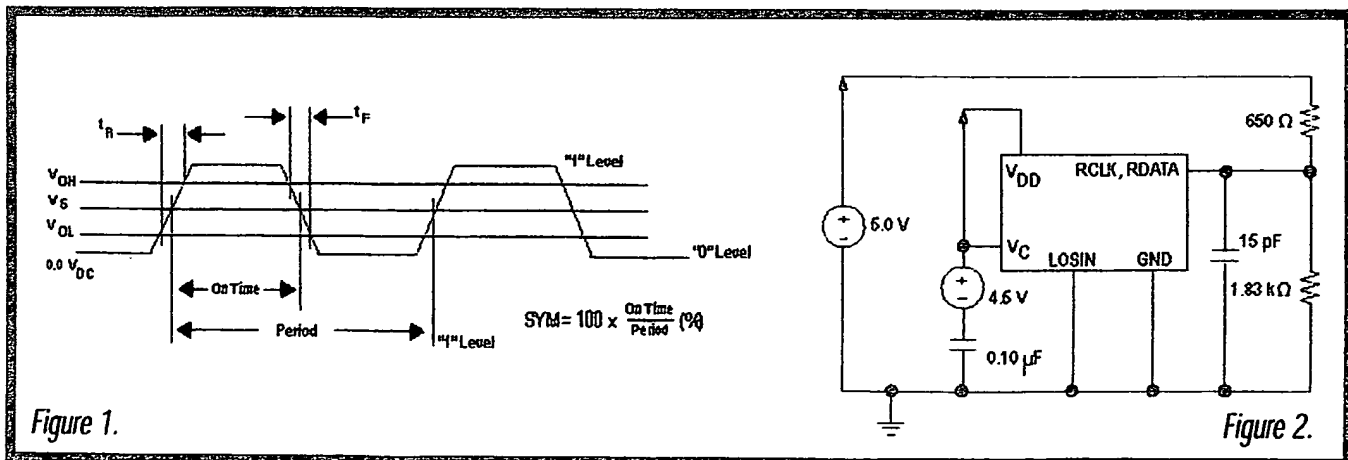
### Note

1. All V<sub>DD</sub> and V<sub>SS</sub> pins must be connected to the same supply.

- For input RZ data, Manchester encoded data, and input clock recovery applications, the output clock must run at two times the input rate to ensure that the input is clocked correctly. Since the output clock has a maximum frequency of 65.536 MHz, these inputs are limited to a maximum rate of 32.768 MHz.
- OUT2 is a binary submultiple of OUT1, or it may be disabled.
- A 3.3 volt supply option is also available.
- Figure 1 defines these parameters. Figure 2 illustrates the equivalent five-gate MTTL load and operating conditions under which these parameters are specified and tested.
- Symmetry is the ON TIME/PERIOD in percent with  $V_S = 1.4$  V for TTL, per Figure 1.
- A loss of signal (LOS) indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.
- Accuracy at room temperature. Stability over temperature is typically  $\pm 20$  ppm.

Parameter	Symbol	Min	Max	Unit
Input NRZ Data Rates	DATAIN	0.008	65.536	MHz
Input RZ Data and Clock Rates <sup>1</sup>	DATAIN	0.008	32.768	MHz
Nominal Output Frequency				
Output 1	OUT1	12.0	65.536	MHz
Output 2 <sup>2</sup>	OUT2	0.05	32.768	MHz
Supply Voltage <sup>3</sup>	V <sub>DD</sub>	4.5	5.5	V
Supply Current (V <sub>DD</sub> = 5.5 V)	I <sub>DD</sub>	25	63	mA
Output Voltage Levels (V <sub>DD</sub> = 4.5 V)				
Output Logic High <sup>4</sup>	V <sub>OH</sub>	2.5	-	V
Output Logic Low <sup>4</sup>	V <sub>OL</sub>	-	0.5	V
Transition Times: <sup>4</sup>				
Rise Time (0.5 V to 2.5 V)	t <sub>R</sub>	0.5	5	ns
Fall Time (2.5 V to 0.5 V)	t <sub>F</sub>	0.5	5	ns
Symmetry or Duty cycle <sup>5</sup>				
Output 1	SYM 1	40	60	%
Output 2	SYM 2	45	55	%
Recovered Clock	R <sub>CLK</sub>	40	60	%
Input Data				
Input Logic High	V <sub>IH</sub>	2.0	-	V
Input Logic Low	V <sub>IL</sub>	-	0.8	V
Control Voltage Bandwidth (-3 dB, V <sub>C</sub> = 2.50 V)	BW	50	-	kHz
Sensitivity @ V <sub>C</sub> = V <sub>O</sub>	$\Delta F/\Delta V_C$	See Figure 11		ppm/V
Loss of Signal Indication <sup>6</sup>				
Output Logic High	V <sub>OH</sub>	2.5	-	V
Output Logic Low	V <sub>OL</sub>	-	0.5	V
Nominal Output Frequency on Loss of Signal: <sup>7</sup>				
Output 1	OUT1	-75 ppm	75 ppm	ppm from fo 1
Output 2	OUT2	-75 ppm	75 ppm	ppm from fo 2
Phase Detector Gain	K <sub>D</sub>	-0.53 x Data Density		V/rad

Table 1.



**RF2703****Absolute Maximum Ratings**

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V <sub>DC</sub>
IF Input Level	500	mV <sub>PP</sub>
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

**Caution!** ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					
IF Frequency Range		0.1 to 250		MHz	T=25°C, V <sub>CC</sub> =3.0V, IF=100MHz, LO=200MHz, F <sub>MOD</sub> =500kHz For IF frequencies below ~2.5MHz, the LO should be a square wave. IF frequencies lower than 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.
Baseband Frequency Range		DC to 50		MHz	
Input Impedance		1200    1pF		Ω	Each input, single-ended
<b>LO</b>					
Frequency					Twice (2x) the IF frequency. For IF frequencies below ~2.5MHz, the LO should be a square wave. IF frequencies lower than 100kHz are attainable if the LO is a square wave and sufficiently large DC blocking capacitors are used.
Level		0.06 to 1		V <sub>PP</sub>	
Input Impedance		500    1pF		Ω	
<b>Demodulator Configuration</b>					
Output Impedance		50    1pF		Ω	IF <sub>IN</sub> =28mV <sub>PP</sub> , LO=200mV <sub>PP</sub> , Z <sub>LOAD</sub> =10kΩ
Maximum Output		1.4		V <sub>PP</sub>	Each output, I <sub>OUT</sub> and Q <sub>OUT</sub>
Voltage Gain		20		dB	Saturated
Noise Figure	22.5	24	25.1	dB	V <sub>CC</sub> =3.0V
		24		dB	V <sub>CC</sub> =5.0V
		35		dB	Single Sideband, IF Input of device reactively matched
		-22		dBm	Single Sideband, 50Ω shunt resistor at IF Input
Input Third Order Intercept Point (IIP <sub>3</sub> )		-11		dBm	V <sub>CC</sub> =3.0V, IF Input of device reactively matched
		-19		dBm	V <sub>CC</sub> =3.0V, 50Ω shunt resistor at IF Input
		-8		dBm	V <sub>CC</sub> =5.0V, IF Input of device reactively matched
		-28		dBm	V <sub>CC</sub> =5.0V, 50Ω shunt resistor at IF Input
I/Q Amplitude Balance		0.1	0.5	dB	V <sub>CC</sub> =5.0V, IF Input of device reactively matched, Z <sub>LOAD</sub> =50Ω
Quadrature Phase Error		≤±1		°	
DC Output		800		mV	V <sub>CC</sub> =3.0V, I <sub>OUT</sub> and Q <sub>OUT</sub> to GND
DC Offset	2.0	2.4	2.8	V	V <sub>CC</sub> =5.0V, I <sub>OUT</sub> and Q <sub>OUT</sub> to GND
		≤10	60	mV	I <sub>OUT</sub> to Q <sub>OUT</sub>

7

QUADRATURE  
DEMODULATORS



<b>Modulator Configuration</b>					$I_{IN} = 28\text{mV}_{pp}$ , $LO = 200\text{mV}_{pp}$ $Z_{LOAD} = 1200\Omega$ Saturated Single Sideband, 1dB Gain Compression. Single Sideband  Unadjusted. Carrier Suppression may be optimized further by adjusting the DC offset level between the A and B inputs.
Maximum Output		200		mV <sub>PP</sub>	
Input Voltage		90		mV <sub>PP</sub>	
Voltage Gain		6		dB	
I/Q Amplitude Balance		0.1		dB	
Quadrature Phase Error		$\leq \pm 1$		°	
Carrier Suppression		25		dBc	
Sideband Suppression		30		dBc	
<b>Power Supply</b>					
Voltage		2.7 to 6		V	Operating limits
Current		8		mA	$V_{CC} = 3.0\text{V}$
	8	10	12	mA	$V_{CC} = 5.0\text{V}$

## 12.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	<b>Supply Voltage</b>					
		PIC16C5X-RC	3.0	—	6.25	V	
		PIC16C5X-XT	3.0	—	6.25	V	
		PIC16C5X-10	4.5	—	5.5	V	
		PIC16C5X-HS	4.5	—	5.5	V	
		PIC16C5X-LP	2.5	—	6.25	V	
D002	VDR	<b>RAM Data Retention Voltage<sup>(1)</sup></b>		1.5*	—	V	Device in SLEEP Mode
D003	VPOR	<b>VDD Start Voltage</b> to ensure Power-on Reset		VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	<b>VDD Rise Rate</b> to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	<b>Supply Current<sup>(2)</sup></b>					
		PIC16C5X-RC <sup>(3)</sup>	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
		PIC16C5X-XT	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
		PIC16C5X-10	—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		PIC16C5X-HS	—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		PIC16C5X-HS	—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
		PIC16C5X-LP	—	15	32	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	IPD	<b>Power-down Current<sup>(2)</sup></b>	—	4.0	12	μA	VDD = 3.0V, WDT enabled
			—	0.6	9	μA	VDD = 3.0V, WDT disabled

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

**US Patent Number:5,946,343 Issued to Schotz**

Item Number 15: DSSS Transmitter, CYLINK SSTX

**NO DATASHEET**

**US Patent Number:5,946,343 Issued to Schotz**

Item Number 16: DSSS Receiver, CYLINK Part# SPECTRE

**NO DATASHEET**

**US Patent Number:5,946,343 Issued to Schotz**

Item Number 17: Mixer, IAM81008

**NO DATASHEET**

**US Patent Number:5,946,343 Issued to Schotz**

Item Number 18: Channel Encoder/Decoder, SRT241203

**NO DATASHEET**

**US Patent Number: 5,946,343 Issued to Schotz**

Item Number 19: Interleaver/De-interleaver, SRT-24INT

**NO DATASHEET**

**US Patent Number:5,946,343 Issued to Schotz**

Item Number 20: Optical Digital Receiver, HK-3131-01

**NO DATASHEET**



**US Patent Number:5,946,343 Issued to Schotz**

Item Number 21: Optical Digital Transmitter, HK-3131-03

**NO DATASHEET**

**US Patent Number:5,946,343 Issued to Schotz**

**Item Number 22: Voltage Controlled Oscillator, M2 D300**

**NO DATASHEET**

# EXHIBIT C

NOTE: A=Altstatt S=Schotz FHSS=Frequency Hopping Spread Spectrum w=with Tx=transmitter

System	Part	Supply Current (in mA)	Size (in inches)	Playtime	Note
<b>Altstatt's Tx</b>					
A(Tx)	BA1404	3	18-pin 0.44 x 0.30		FM Stereo Transmitter
				16+ hours	Tx continuous operation time
<b>Schotz FHSS Tx</b>					
S(Tx w SS)	DSP56002	90	144-pin 0.78 x 0.78		PLL located inside DSP56002
	>PLL	1	N/A		ckout located inside DSP56002
	>ckout	14	N/A		
	SAA7360		44-pin 0.50 x 0.50		A/D converter
	>analog	43			function of the A/D converter
	>digital	50			function of the A/D converter
	SAA2520	82	44-pin 0.55 x 0.55		Stereo Filter MPEG
	SAA2521	25	44-pin 0.55 x 0.55		MPEG
	RF2422	45	16-pin 0.39 x 0.24		Modulator
	TQ9132	85	8-pin 0.19 x 0.23		Power Amp
	MC12210	10.2	16-pin 0.39 x 0.24		PLL
	SMV2500	19	12-pin 0.28 x 0.28		VCO
	HK-3131-01	no data	no data		Optical Digital Rcvr (*)
	M2 D300	no data	no data		VCO (*)
	SRT241203	no data	no data		FEC (*)
	SRT-24INT	no data	no data		Interleaver (*)
				0.1 hours or 6+ minutes	
<b>A(Tx) equation in hours:</b>					
$((60 \times 50 \text{ mA-minutes}) / ((60 \text{ minutes/hour} \times 24 \text{ hour/day}) (3 \text{ mA}))) \times (24 \text{ hour/day}) = 16.6 \text{ hours}$					
<b>S(Tx w SS) equation in hours:</b>					
$((60 \times 50 \text{ mA-min.}) / ((60 \text{ min./hr} \times 24 \text{ hr/day}) (90 + 1 + 14 + 43 + 50 + 82 + 25 + 45 + 85 + 10.2 + 19 \text{ mA}))) \times (24 \text{ hr/day}) = 6.4 \text{ min}$					
where min = minutes and hr = hours					
(*) = Unable to locate datasheet for integrated chip (IC) referenced by Schotz					

NOTE : A=Altstatt S=Schotz FHSS=Frequency Hopping Spread Spectrum w=with Rx=Receiver

System	Part	SupplyCurrent (in mA)	Size (in inches)	Playtime	Note
					Altstatt's Rx
A(Rx)	TA7792	4	16-pin 0.77 x 0.30		AM/FM Tuner System
	TA7766A	0.8	18-pin 0.44 x 0.30		FM PLL
				10+ hours	Rx continuous operation time

S(Rx w SS)	DSP56002	90	144-pin 0.78 x 0.78		Schotz FHSS Rx
	>PLL	1	N/A		PLL located inside DSP56002
	>ckout	14	N/A		ckout located inside DSP56002
	MGA86576	16	4-pin 0.20 x 0.07		LNA
	HK-3131-03	no data	no data		Optical Digital Tx (*)
	CS8402	1.5	28-pin 1.20 x 0.20		Digital Interface Tx
	SAA2520	82	44-pin 0.55 x 0.55		Stereo Filter MPEG
	TDA1305T	42	28-pin 0.70 x 0.40		DAC
	TRU-050	63	16-pin 0.80 x 0.30		Clock Recovery and Timing
	RF2703	10	14-pin 0.34 x 0.24		Demodulator
	MC12210	10.2	16-pin 0.39 x 0.24		PLL
	SMV2500	19	12-pin 0.28 x 0.28		VCO
	SRT241203	no data	no data		FEC (*)
	SRT-24INT	no data	no data		De-interleaver (*)
	IAM81008	no data	no data		Mixer (*)
				0.14 hours or 8+ minutes	

A(Rx) equation in hours:

$$\{((60 \times 50 \text{mA} \cdot \text{minutes}) / ((60 \text{ minutes/hour} \times 24 \text{ hour/day})(4.8 \text{mA})))\} \times (24 \text{ hour/day})$$

S(Rx w SS) equation in hours:

$$\{((60 \times 50 \text{mA} \cdot \text{minutes}) / ((60 \text{ minutes/hour} \times 24 \text{ hour/day})(\text{sum of IC currents in mA})))\} \times (24 \text{ hour/day})$$

(\*) = Unable to locate datasheet for integrated chip (IC) referenced by Schotz

NOTE : A=Altstatt S=Schotz DSSS=Direct Sequence Spread Spectrum w=with Tx=transmitter

System	Part	SupplyCurrent (in mA)	Size (in inches)	Playtime	Note
					Altstatt's Tx
A(Tx)	BA1404	3	18-pin 0.44 x 0.30		FM Stereo Transmitter
				16+ hours	Tx continuous operation time
S(Tx w SS)	DSP56002	90	144-pin 0.78 x 0.78		Schotz DSSS Tx
	>PLL	1	N/A		PLL located inside DSP56002
	>ckout	14	N/A		ckout located inside DSP56002
	PIC16C55	1.8	28-pin 1.5 x 0.50		Microprocessor
	SAA7360		44-pin 0.50 x 0.50		A/D converter
	>analog	43			function of the A/D converter
	>digital	50			function of the A/D converter
	RF2422	45	16-pin 0.39 x 0.24		Modulator
	MC12210	10.2	16-pin 0.39 x 0.24		PLL
	SMV2500	19	12-pin 0.28 x 0.28		VCO
	CYLINK SSTS	no data	no data		DSSS Transmitter (*)
	HK-3131-01	no data	no data		Optical Digital Rcvr (*)
	M2 D300	no data	no data		VCO (*)
				0.18 hours or 11 minutes	
A(Tx) equation in hours:					
$\{(60 \times 50 \text{mA-minutes}) / [(60 \text{ minutes/hour} \times 24 \text{ hour/day})(3 \text{mA})]\} \times (24 \text{ hour/day})$					
S(Tx w SS) equation in hours:					
$\{(60 \times 50 \text{mA-minutes}) / [(60 \text{ minutes/hour} \times 24 \text{ hour/day})(\text{sum of IC currents in mA})]\} \times (24 \text{ hour/day})$					
(*) = Unable to locate datasheet for integrated chip (IC) referenced by Schotz					

NOTE : A=Altstatt S=Schotz DSSS=Direct Sequence Spread Spectrum w=with Rx=Receiver

System	Part	SupplyCurrent (in mA)	Size (in inches)	Playtime	Note
					Altstatt's Rx
A(Rx)	TA7792	4	16-pin 0.77 x 0.30		AM/FM Tuner System
	TA7766A	0.8	18-pin 0.44 x 0.30		FM PLL
				10+ hours	Rx continuous operation time

S(Rx w SS)	DSP56002	90	144-pin 0.78 x 0.78		Schotz DSSS Rx
	>PLL	1	N/A		PLL located inside DSP56002
	>ckout	14	N/A		ckout located inside DSP56002
	PIC16C55	1.8	28-pin 1.5 x 0.50		Microprocessor
	CYLINK	no data	no data		DSSS Receiver
	MGA86576	16	4-pin 0.20 x 0.07		LNA
	IAM81008	no data	no data		Mixer (*)
	CS8402	1.5	28-pin 1.20 x 0.20		Digital Interface Tx
	TDA1305T	42	28-pin 0.70 x 0.40		DAC
	MC12210	10.2	16-pin 0.39 x 0.24		PLL
	SMV2500	19	12-pin 0.28 x 0.28		VCO
	HK-3131-03	no data	no data		Optical Digital Tx (*)
				0.25 hours or 15 minutes	

A(Rx) equation in hours:

$$\{(60 \times 50 \text{mA} \cdot \text{minutes}) / [(60 \text{ minutes/hour} \times 24 \text{ hour/day})(4.8 \text{mA})]\} \times (24 \text{ hour/day})$$

S(Rx w SS) equation in hours:

$$\{(60 \times 50 \text{mA} \cdot \text{minutes}) / [(60 \text{ minutes/hour} \times 24 \text{ hour/day})(\text{sum of IC currents in mA})]\} \times (24 \text{ hour/day})$$

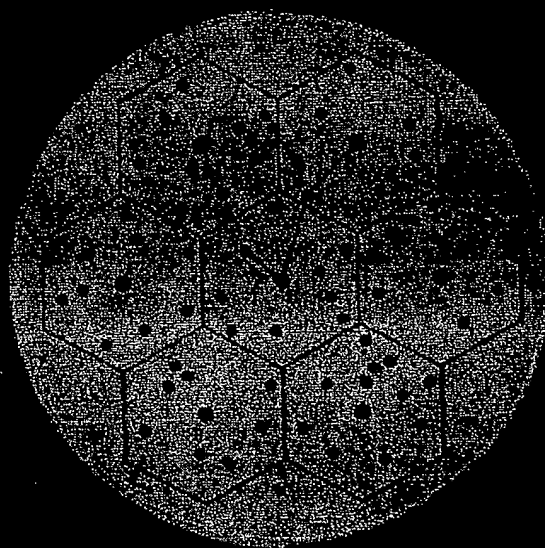
(\*) = Unable to locate datasheet for integrated chip (IC) referenced by Schotz

EXHIBIT D

# WIRELESS

communications

Principles  Practice



Theodore S. Rappaport

microcellular systems. However, satellite mobile systems offer tremendous promise for paging, data collection, and emergency communications, as well as for global roaming before IMT-2000 is deployed. In early 1990, the aerospace industry demonstrated the first successful launch of a small satellite on a rocket from a jet aircraft. This launch technique is more than an order of magnitude less expensive than conventional ground-based launches and can be deployed quickly, suggesting that a network of LEOs could be rapidly deployed for wireless communications around the globe. Already, several companies have proposed systems and service concepts for worldwide paging, cellular telephone, and emergency navigation and notification [IEE91].

In emerging nations, where existing telephone service is almost nonexistent, fixed cellular telephone systems are being installed at a rapid rate. This is due to the fact that developing nations are finding it is quicker and more affordable to install cellular telephone systems for fixed home use, rather than install wires in neighborhoods which have not yet received telephone connections to the PSTN.

The world is now in the early stages of a major telecommunications revolution that will provide ubiquitous communication access to citizens, wherever they are [Kuc91], [Goo91], [ITU94]. This new field requires engineers who can design and develop new wireless systems, make meaningful comparisons of competing systems, and understand the engineering trade-offs that must be made in any system. Such understanding can only be achieved by mastering the fundamental technical concepts of wireless personal communications. These concepts are the subject of the remaining chapters of this text.

## 1.6 Problems

- 1.1 Why do paging systems need to provide low data rates? How does a low data rate lead to better coverage?
- 1.2 Qualitatively describe how the power supply requirements differ between mobile and portable cellular phones, as well as the difference between pocket pagers and cordless phones. How does coverage range impact battery life in a mobile radio system?
- 1.3 In simulcasting paging systems, there usually is one dominant signal arriving at the paging receiver. In most, but not all cases, the dominant signal arrives from the transmitter closest to the paging receiver. Explain how the FM capture effect could help reception of the paging receiver. Could the FM capture effect help cellular radio systems? Explain how.
- 1.4 Where would walkie-talkies fit in Tables 1.5 and 1.6? Carefully describe the similarities and differences between walkie-talkies and cordless telephones. Why would consumers expect a much higher grade of service for a cordless telephone system?
- 1.5 Assume a 1 Amp-hour battery is used on a cellular telephone (often called a cellular subscriber unit). Also assume that the phone's radio receiver draws 35 mA on receive and 250 mA during a call. How long would the phone work (i.e. what is the battery life) if the user has one 3-minute call every day? every 6



hours? every hour? What is the maximum talk time available on the cellular phone in this example?

- 1.6 Assume a CT2 subscriber unit has the same size battery as the phone in Problem 1.5, but the paging receiver draws 5 mA and the transmitter draws 80 mA during a call. Recompute the battery life for the cases in Problem 1.5. Recompute the maximum talk time for the CT2 handset.
- 1.7 Why would one expect the CT2 handset in Problem 1.6 to have a smaller battery drain during transmission than a cellular telephone?
- 1.8 Why is FM, rather than AM, used in most mobile radio systems today? List as many reasons as you can think of, and justify your responses. Consider issues such as fidelity, power consumption, and noise.
- 1.9 List the factors that led to the development of (a) the GSM system for Europe, and (b) the U.S. digital cellular system. How important was it for both efforts to (i) maintain compatibility with existing cellular phones? (ii) obtain spectral efficiency? (iii) obtain new radio spectrum?
- 1.10 Assume that a GSM, an IS-95, and a U.S. digital cellular base station transmit the same power over the same distance. Which system will provide the best SNR at a mobile receiver? How much is the improvement over the other two systems? Assume a perfect receiver with only thermal noise is used for each of the three systems.
- 1.11 Discuss the similarities and difference between a conventional cellular radio system and a space-based cellular radio system. What are the advantages and disadvantages of each system? Which system could support a larger number of users for a given frequency allocation? How would this impact the cost of service for each subscriber?
- 1.12 Assume that wireless communication services can be classified as belonging to one of the following four groups:
  - High power, wide area systems (cellular)
  - Low power, local area systems (cordless telephone and PCS)
  - Low speed, wide area systems (mobile data)
  - High speed, local area systems (wireless LANs)Classify each of the wireless systems described in Chapter 1 using these four groups. Justify your answers. Note that some systems may fit into more than one group.
- 1.13 Discuss the importance of regional and international standards organizations such as ITU-R, ETSI, and WARC. What competitive advantages are there in using different wireless standards in different parts of the world? What disadvantages arise when different standards and different frequencies are used in different parts of the world?
- 1.14 Based on the proliferation of wireless standards throughout the world, discuss how likely it is for IMT-2000 to be adopted. Provide a detailed explanation, along with probable scenarios of services, spectrum allocations, and cost.

**Solutions Manual to Accompany**

**Wireless Communications  
Principles and Practices**  
FIRST EDITION

**Zhigang Rong**

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infrastructure, complexity, hardware cost are all low.

A cordless telephone, on the

other hand, is a full duplex system. It allows simultaneous two-way communication. Transmission and reception uses two different channels (FDD) although new cordless systems are using TDD. The coverage range, required infrastructure, hardware cost of a cordless phone system are low and the complexity is moderate. User expectations are higher for a cordless telephone.

1.5 If the user has one 3-minute call every day

$$\begin{aligned} \text{the battery life} &= \frac{60 \times 1000 \text{ (mA-minute)}}{(60 \times 24 - 3) \times 35 + 3 \times 250 \text{ (mA-minute)}} \\ &\doteq 1.175 \text{ days} \doteq \underline{\underline{28.2 \text{ hours}}} \end{aligned}$$

the user has one 3-minute call every 6 hours

$$\text{the battery life} = \frac{60 \times 1000}{(60 \times 6 - 3) \times 35 + 3 \times 250} \times 6 \doteq \underline{\underline{27.18 \text{ hours}}}$$

If the user has one 3-minute call every hour.

$$\text{the battery life} = \frac{60 \times 1000}{(60 - 3) \times 35 + 3 \times 250} \doteq \underline{\underline{21.86 \text{ hours}}}$$

$$\text{the maximum talk time} = \frac{60 \times 1000}{250} = 240 \text{ minutes} = \underline{\underline{4 \text{ hours}}}$$

1.6 For 3-minute call/day

$$\text{battery life} = \frac{60 \times 1000 \text{ (mA-minute)}}{(60 \times 24 - 3) \times 35 + 3 \times 80} \doteq 8.08 \text{ days} = \underline{\underline{193.94 \text{ hours}}}$$

1.6 Cont'd

For 3 minute-call / 6 hours,

$$\text{battery life} = \frac{60 \times 1000}{(60 \times 6 - 3) \times 35 + 3 \times 80} \times 6 \doteq \underline{\underline{177.78 \text{ hours}}}$$

For 3 minute-call / hour,

$$\text{battery life} = \frac{60 \times 1000}{(60 - 3) \times 35 + 3 \times 80} \doteq \underline{\underline{114.29 \text{ hours}}}$$

$$\text{The maximum talk time} = \frac{60 \times 1000}{80} = 750 \text{ minutes} = \underline{\underline{12.5 \text{ hours}}}$$

1.7 Since the coverage range of the CT-2 system is lower

than that of the cellular radio system, to obtain the same signal-to-noise ratio in the coverage area, a CT-2 handset requires less transmitted power than a cellular telephone, and thus a smaller battery drain.

1.8 FM has several advantages over AM. The most important

advantage is FM's superior noise suppression characteristics. With conventional AM, the modulating signal is impressed onto the carrier in the form of amplitude variations. However, noise introduced into the system also produces changes in the amplitude of the envelope. Therefore, the noise cannot be removed from the composite waveform without also removing a portion of the information signal. With FM, the information is impressed onto the carrier in the form of frequency variations. Therefore, with FM receivers,

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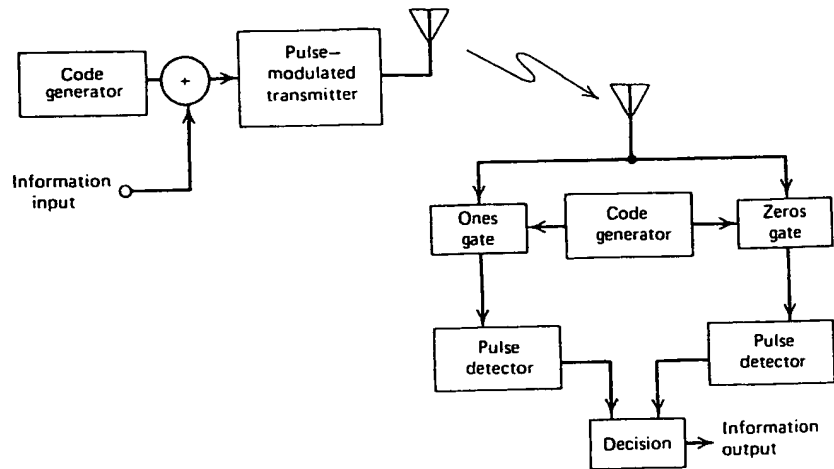


Figure 2.23 Simple time-hopping (pseudorandom pulse) system.

time-frequency hopping system might change frequency and/or amplitude only at one/zero transitions in the code sequence. Figure 2.23 shows a time-hopping system in block form. The simplicity of the modulator is obvious. Any pulse-modulatable signal source capable of following code waveforms is eligible as a time-hopping modulator.

Time hopping may be used to aid in reducing interference between systems in time-division multiplexing. However, stringent timing requirements must be placed on the overall system to ensure minimum overlap between transmitters. Also, as in any other coded communications system, the codes must be considered carefully from the standpoint of their cross-correlation properties.

Simple time-hopping modulation offers little in the way of interference rejection because a continuous carrier at the signal center frequency can block communications effectively. The primary advantage offered is in the reduced duty cycle; that is, to be really effective an interfering transmitter would be forced to transmit continuously (assuming the coding used by the time-hopper is unknown to the interferer). The power required of the reduced-duty-cycle time-hopper would be less than that of the interfering transmitter by a factor equal to the signal duty cycle.

Because of this relative vulnerability to interference, simple time-hopping transmissions should not be used for antijamming unless combined with frequency hopping to prevent single frequency interferers from causing significant losses. For ranging, multiple access, or other special uses time-hopping may be especially useful, if only because of the simplicity of generating the transmitted signal.

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